REMARKS

The Office Action issued on July 11, 2007, has been received, assessed, and addressed in its entirety, as detailed below. Accordingly, Applicants assert that the present Response is fully responsive to the Office Action, and respectfully request reconsideration of the rejection set forth therein based upon the following points. Claims 1-5 are pending for consideration, of which claim 1 is independent.

Claims 1-5 stand rejected under 35 U.S.C. §102(b) as anticipated by Sano et al. (US2004/0107408). Applicants respectfully traverse this rejection for at least the following reasons.

Independent claim 1 recites a method of designing a semiconductor integrated circuit including first, second, and third step for verifying of a circuit design of the semiconductor integrated circuit, wherein "at least the first and second steps are performed *prior to a layout design of the semiconductor integrated circuit*," (emphasis added). In direct contrast to Applicants' claimed invention, Sano et al. explicitly requires simultaneous circuit and logic component layout design. Specifically, Sano et al. is directed toward incorporating floor plan information with regard to clustering of flip-flop cells with designs for constructing a clock tree. As shown in FIG. 21, and cited by the Office as providing evidence of anticipation of Applicant's claimed invention, Sano et al. explicitly discloses an outline of an LSI layout designing method (circuit designing method) that includes simultaneous component layout design. For example, Sano et al. explicitly discloses (paragraph [0260]):

> "Then, at step S122, an initial placement is tried to arrange for only the flip-flop cells connected to a data line so that the floorplan information is utilized and the clock path extracted at step S121 is disregarded."

In addition, Sano et al. explicitly discloses (paragraphs [0263] to [0267]) specific consideration of requirements regarding placement restriction area information and cluster information for flip-flop cells, as well as trying and re-trying placement of the flip-flop cells. Moreover, Sano et al. explicitly discloses various diagrams in FIGs. 26-35 and 37-40, for example, for consideration of flip-flop cell placement during the circuit designing method. Accordingly, Sano et al. is explicitly directed toward a method of simultaneously performing circuit design and component layout design. Thus, Applicants respectfully assert that Sano et

al. is completely silent with regard to a method of designing a semiconductor integrated circuit including first, second, and third step for verifying of a circuit design of the semiconductor integrated circuit, wherein "at least the first and second steps are performed prior to a layout design of the semiconductor integrated circuit," as required by independent claim 1, and hence dependent claims 2-5.

With regard to claims 2-5, Applicants respectfully assert that claims 2-5 are also allowable for at least the combination of features each of claims 2-5 recite, as well as their dependence upon independent claim 1.

For the reasons presented above, since each and every feature of at least independent claim 1 is neither taught nor suggested by Sano et al., as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1-5, under 35 U.S.C. §102(b) as being anticipated by Sano et al. is improper and should be withdrawn.

In view of the arguments set forth above, Applicants respectfully request reconsideration and withdrawal of the pending rejection, and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,

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